(Pages : 2) **1501**

Reg. No. : .....

Name : .....

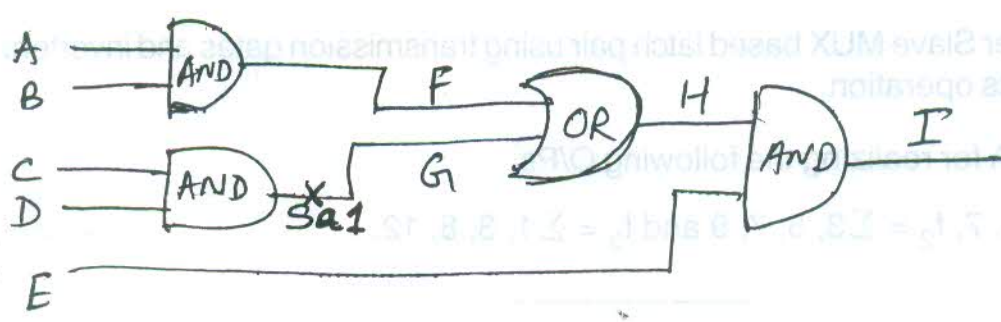
Sixth Semester B.Tech. Degree Examination, April 2014
(2008 Scheme)
08.602 : VLSI DESIGN (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. What are positive and negative photo resists ? Explain.
2. Explain how capacitors and resistors are fabricated on an IC chip.
3. What are the important factors to be considered in multilevel metallization ? Explain.
4. Explain substrate bias effect in MOSFETS. What are the parameters that will affect the body factor of a MOSFET device ?
5. What are oxide related capacitances and junction capacitances ?
6. What is np-cmos ? Explain the properties of np-cmos.
7. Draw the circuit diagram of a transmission gate XOR logic and explain its operation.
8. Using path sensitization method find the input pattern that detects the stuck at fault shown in the figure.



P.T.O.

9. Design a 4×4 NOR ROM and explain its working.

10. Explain the working of a 1-Transistor DRAM cell with the help of timing diagrams.

PART – B

Answer **two** questions from **each** module. **Each** question carries **10** marks.

Module – I

11. Briefly explain with the help of necessary diagrams, p-n junction isolation and dielectric isolation methods.

12. Explain the photolithographic sequence of IC fabrication with the help of necessary diagrams.

13. Draw the cross sectional layout view of a SOI MOSFET structure and list its advantages over bulk MOSFET and its applications.

Module – II

14. With the help of an adder example explain the VLSI design flow from specifications to physical level representation.

15. What is scaling ? Explain constant field, constant voltage and generalized scaling methods.

16. What are the advantages and disadvantages of dynamic logic ? Draw the dynamic logic circuit of a NAND gate and explain its operation.

Module – III

17. Design a 14 bit square root carry select adder. Calculate the worst case delay.

18. Draw a Master Slave MUX based latch pair using transmission gates and inverters and explain its operation.

19. Design a PLA for realizing the following O/Ps

    $f_1 = \Sigma 1, 2, 6, 7$, $f_2 = \Sigma 3, 5, 7, 9$ and $f_3 = \Sigma 1, 3, 8, 12$.
